Novel Power-grid Design & Layout Strategy for SoC ESD-CDM Robustness

Authors : Villy Gohil ; Karthik Kodakandla ; MuraliMohan Thota ; Subhadeep Ghosh

Company : Texas Instruments

Problem Statement

Along with meeting the design's IR drop without creating congestion, the electro-static discharge (ESD) perspective is also an important dimension of power grid and layout signoff tested by the charged-device model (CDM) qualification.

This makes it imperative for designers to address ESD-CDM while not penalizing other design closure aspects like EM,IR.

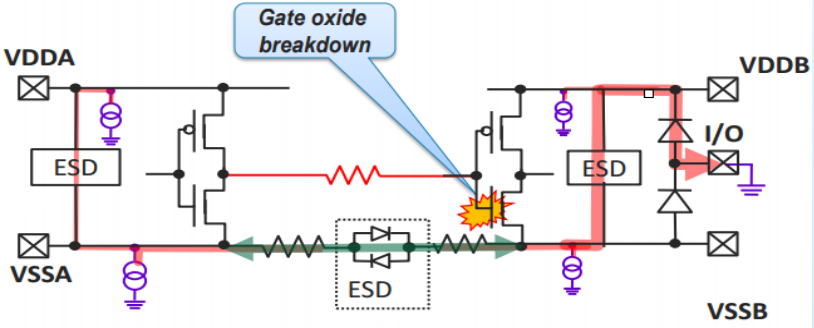


Fig. 1 Gate-Oxide breakdown - due to high Differential Voltage. For same domain, assume VSSA, VSSB as VSS, VDDA, VDDB as VDD, no diode structure in green path.

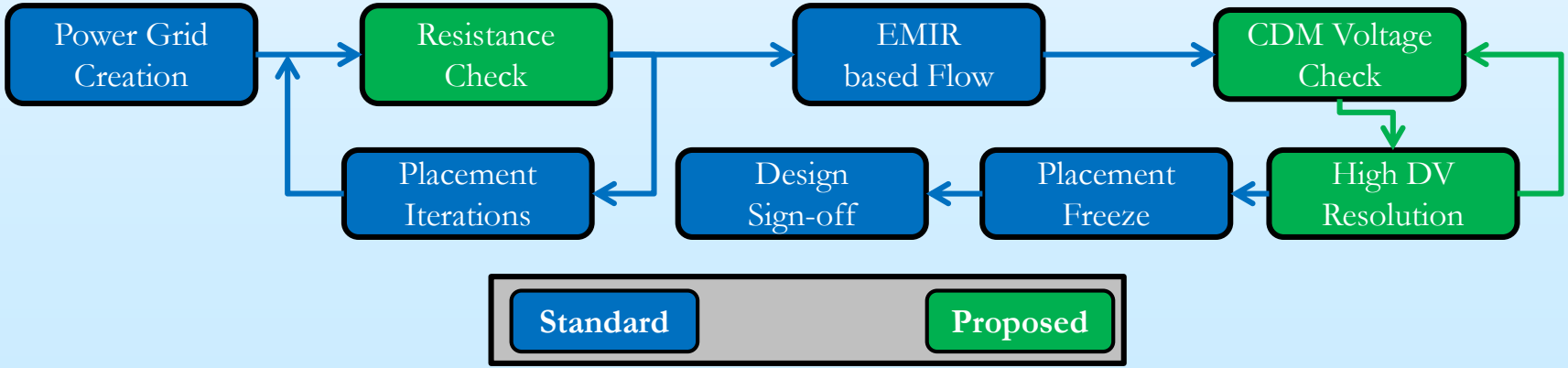
In CDM testing, complete package is charged & the discharge is channeled through each pin separately, hence, the discharge path involves the core standard cell area i.e., charge flows from substrate, power-rails to straps to power/ground pads and finally through zapped pin via CDM structures.

There might be a potential difference developed across driver-receiver (Dr-Rc) pairs during transient discharge due to unequal current flow for reasonable amount of time leading to gate-oxide break down, refer Fig. 1.

Motivation is to develop a novel power grid and layout closure methodology to address high differential voltages

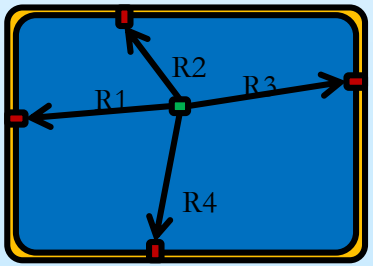
Proposed Methodology

- The proposed methodology addresses CDM-ESD perspective and has following fundamental properties – available early in the design phase, fairly independent of placement iterations & co-relates well with final ESD signoff results.
- Resistance is a indicator of grid strength and also plays a pivotal role in ESD & IR performance of the SoC. Resistance check of each and every cell present on the die, independent of the cell type followed by systematic grouping and identifying trends could be used to find out regions on SoC with weak (high resistive) supply
- CDM Voltage Check is performed to validate presence of Dr-Rc pairs with high differential voltage(DV). Integrating resistance check early in the design flow would help us predictably avoid DV/IR hotspots and using CDM Voltage Check towards the end would help us signoff the design efficiently.
- **AR → Resistance Check ; DV → CDM Voltage Check**
- Since this methodology involves resistance check early in the design phase, it reduces the design scenarios with high differential voltage, which would otherwise prove tedious to address due to design maturity.



AR & DV Flows

- Resistance and CDM Voltage Checks by nature do not have fixed thresholds for declaring violations. We use histograms as means to analyze and declare soft thresholds and work by clearing outliers.
- Using Resistance Check we identify regions with weak power supply and then decide upon the action plan to address these regions on the basis of following factors:
  - Importance of the region (like near some timing critical IPs) → This is the highest priority
  - Amount of metal resources required to improve supply in the region → If not causing congestion, improve supply
  - Digital area gained if we do not block the region for standard cell placement → May block high resistive areas partially
- CDM Voltage Check done on real design has specifically highlighted 4 generic cases showing high DV:
  - Dr-Rc pair far apart on die → Add a buffer cell or reduce physical distance between the Dr-Rc
  - Dr-Rc pair sitting along a channel → Reduce number of cells or increase supply strength in the channel
  - Core cell & IO as Dr-Rc → Improve mutual connectivity between supplies of IO & core cell
  - Dr-Rc pair across a macro → Add a buffer cell or improve supply mutual connectivity across the macro



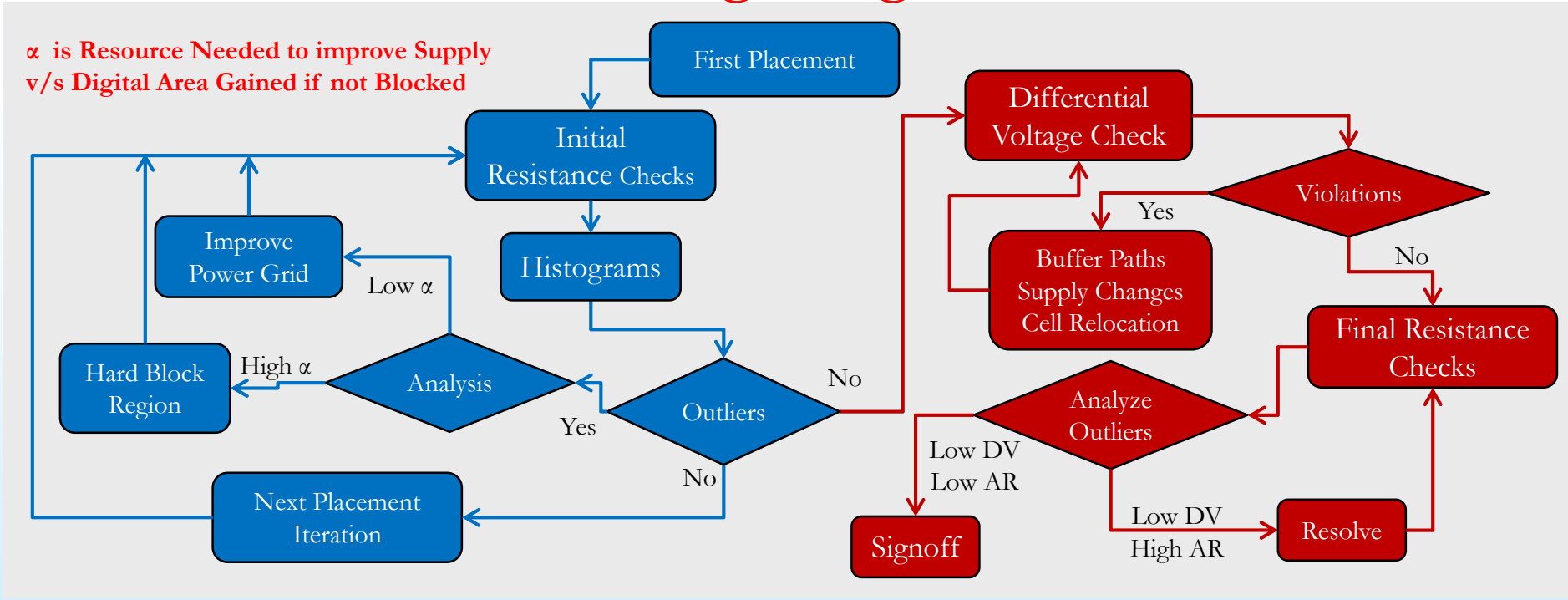
→ Pads

→ Core Cell

$AR = R_{eff}(R1, R2, R3, R4)$

where, R_{eff} *is resistance obtained by shorting PADs at top level*

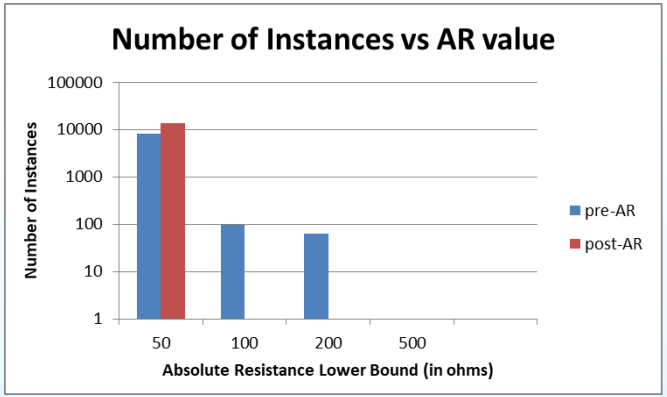
Power Grid ESD flow integrating AR and DV

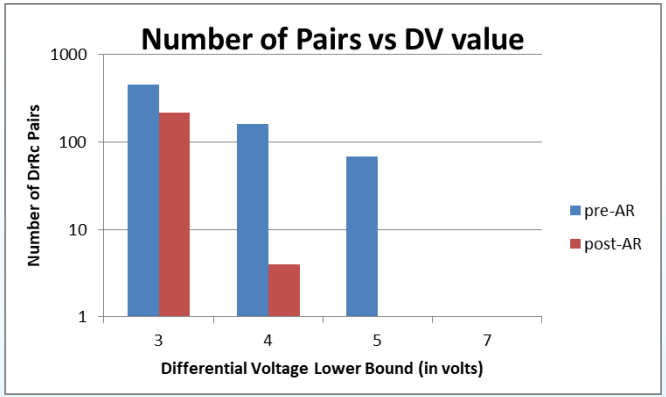


This combination of Power Grid iterations based on AR followed up by final closure with DV creates a robust, efficient and usable flow to close the design.

Early **Final**

Design Case





- Above graphs illustrate results seen on a real design. Blue Bar Graph represents number of instances at DV/AR values on a non-AR optimized DB & Red Bar Graph, the same on an AR optimized DB.
- High count of DV violations seen in the pre-AR DB have been predictably avoided on the post-AR DB.
- The first AR resolved DB of one of the real design, with fully functional setup showed ZERO DV violations defined by the respective technology rules. This dictates the strength and foresight provided by AR flow in resolution of DV violations.

Summary

- **AR detects weak power grid** irrespective of the type of cell present in a given location while, **DV detects the voltage build-up** with a Dr-Rc pair information in a given location. This makes AR an exhaustive flow, while with only DV, we would always be at risk of seeing variation in results across iterations.
- Since, **AR is an exhaustive region oriented flow**, it filters most of the cases to be solved by **changing power grid early in the design**, this leaves behind mostly the cases to be resolved by buffer addition or cell relocation.
- Insightful ordering of the flows gives **a strategic advantage in efficiently resolving/reducing the DV violations** and their count. Each DV violation has a fixed plan of action and provides liberty for generating automated flows for resolving the violations.
- The **combination of Power Grid iterations based on AR followed up by final closure with DV** creates a robust, efficient and usable flow to close the power grid and layout.